AMENDMENTS TO THE SPECIFICATION

Please delete the paragraph appearing at page 7, line 22, through page 8, line 10, and insert therefor:

FIGURE 5 shows a linearized, hybrid, Z-Transform model of a MASH fourth-order delta-sigma modulator. Each stage of delta-sigma modulator typically comprises summer 50, quantizer 51, summer 52, which usually subtracts the intermediate digitized signal, and delay 53, represented in Z-Transform notation. The second through fourth stages also generally include a number of digital differentiators 54, represented in Z-Transform notation, corresponding to the stage level minus one. Therefore, stage two modulator 520 typically contains one digital differentiator 54 (i.e., 2 - 1 = 1), while stage four modulator 540 typically contains three digital differentiators 54 (i.e., [[3 - 1 = 2]] 4 - 1 = 3). These cascaded digital differentiators usually shape the quantization noise of each stage prior to the final summing in summer 500. The noise canceling characteristics of the MASH architecture can generally be observed through mathematically processing a theoretical signal through delta-sigma modulator system 5. The digitized output signal of delta-sigma modulator system 5 typically comes from summer 500. The intermediate digitized output signals from each of the delta-sigma modulator stages are generally added together at summer 500 to form the final modulated output signal. From stage one modulator 510, stage one digitized signal A1 may be mathematically represented by the following formula: